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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/592,207	NAGARASA ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to the amendment filed June 4, 2004. Claims 1-13 and 15-23 are pending.

2. Applicant's arguments with respect to claims 1-13 and 15-23 have been considered but are moot in view of the new ground(s) of rejection.

Specification

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. The specification is objected to under 35 U.S.C. 112, first paragraph, as failing to support the subject matter set forth in the claims. The specification, as originally filed does not provide support for the invention as now claimed.

The test to be applied under the written description portion of 35 U.S.C. 112, first paragraph, is whether the disclosure of the application as originally filed reasonably conveys to the artisan that the inventor had possession at that time of later claimed subject matter. Vas-Cat, Inc. v. Mahurkar, 935 F. 2d 1555, 1565, 19 USPQ2d 111, 1118 (Fed. Cir. 1991), reh'rg denied (Fed. Cir. July 8, 1991) and reh'rg, en banc, denied (Fed. Cir. July 29, 1991).

The amended claims include the limitations "wherein a total of all of said plurality of delay times is less that said period of said clock signal". However, the specification does not provide an enabling disclosure support these claimed limitations.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 21 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular the claim was previously amended to include the limitation "wherein a total of all of said plurality of delay times is less that said period of said clock signal". This constitutes new matter that is not described by the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 11-13, 15-21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Conn et al., U.S. Patent No. 6,150,863 (hereinafter "Conn"), in view of Dallas Semiconductor Datasheet, "DS1020 Programmable 8-Bit Silicon Delay Line", November 17, 1999 (hereinafter "Dallas").

As per claim 1, Conn teaches an apparatus comprising:

a first input configured to receive a clock signal (Fig. 5, pin CK of flip-flop 510A);

a second input configured to receive a data signal having a first setup/hold window with respect to a transition of said clock signal (I/O pad 220A);

a first circuit (delay circuit 210A) configured to

(i) receive said data signal from said second input (via I/O pad 220A) and

(ii) present a delayed data signal (via line 260A) having a second setup/hold window with respect to said transition of said clock signal (Col. 5, lines 45-58), wherein

(i) a difference between said first setup/hold window and said second setup/hold window is configured in response to one or more of a plurality of delay times (Fig. 2, delay elements 240-246), and

(ii) said plurality of delay times provides a user configurable delay of said second setup/hold window relative to said transition of said clock signal (Col. 5, lines 65-67); and

a second circuit configured to receive said delayed data signal from said first circuit and said clock signal from said first input (flip-flop 510A).

However, while Conn teaches a sample absolute value of the delay times and that the delay times may be modified (Col. 3, lines 45-60), Conn is silent regarding the size of the delay times in comparison with the period of a clock signal. Dallas teaches a programmable delay in which each of said plurality of delay times is less than a period of a clock signal (Table 2 on page 4, maximum delay for DS1020-15 is 48.25 ns; AC Electrical Characteristics on page 6, minimum clock width is 50 ns). At the time of the invention, it would have been obvious to apply the details of Dallas' programmable delay to Conn's apparatus. A motivation for doing so would have been to "to satisfy the requirements of a particular application" (Conn, Col. 3, lines 45-60).

As per claim 2, Conn further teaches said second circuit is configured to present a data output (via Q pin) in response to said delayed data signal and said clock signal.

As per claim 3, Conn teaches that said second circuit functions as a register that is further configured to store said delayed data signal in response to said clock signal (Col. 1, lines 60-61, flip-flop functions as a register)

As per claim 21, Dallas teaches a total of all of said plurality of delay times is less than said period of said clock signal (Table 2 on page 4, maximum delay for DS1020-15 is 48.25 ns; AC Electrical Characteristics on page 6, minimum clock width is 50 ns).

As per claim 23, Conn teaches said data signal and said clock signal are externally generated (Fig. 5, external to elements 220A, 210A, and 510A).

As per claim 11, Conn teaches an apparatus comprising:

means for receiving (i) a clock signal and (ii) a data signal having a first setup/hold window with respect to a transition of said clock signal (Fig. 5, pin CK of flip-flop 510A; I/O pad 220A);

means for presenting a delayed data signal having a second setup/hold window with respect to said transition of said clock signal in response to said data signal (delay circuit 210A), wherein

(i) a difference between said first setup/hold window and said second setup/hold window is configured in response to one or more of a plurality of delay times (Fig. 2, delay elements 240-246), and

(ii) said plurality of delay times provides a user configurable delay of said second setup/hold window relative to said transition of said clock signal (Col. 5, lines 65-67); and

means for storing said delayed data signal in response to said clock signal (flip-flop 510A).

However, while Conn teaches a sample absolute value of the delay times and that the delay times may be modified (Col. 3, lines 45-60), Conn is silent regarding the size of the delay times in comparison with the period of a clock signal. Dallas teaches a programmable delay in which each of said plurality of delay times is less than a period of a clock signal (Table 2 on page 4, maximum delay for DS1020-15 is 48.25 ns; AC Electrical Characteristics on page 6, minimum clock width is 50 ns). At the time of the invention, it would have been obvious to apply the details of Dallas' programmable delay to Conn's apparatus. A motivation for doing so would have been to "to satisfy the requirements of a particular application" (Conn, Col. 3, lines 45-60).

As per claim 12, Conn teaches a method for programming a setup/hold window, comprising the steps of:

(A) receiving (i) a clock signal and (ii) a data signal having a first setup/hold window with respect to a transition of said clock signal (Fig. 5, from DLY 530 and I/O pad 220A); and

(B) presenting

(i) a delayed data signal (via line 260A) (a) having a second setup/hold window with respect to said transition of said clock signal (Col. 5, lines 45-58) and (b) generated in response to said data signal to a first input of a circuit (pin D of flip-flop 510A) and

(ii) said clock signal to a second input of said circuit (pin CK of flip-flop 510A), wherein

(i) a difference between said first setup/hold window and said second setup/hold window is configured in response to one or more of a plurality of delay times (Fig. 2, delay elements 240-246), and

(ii) said plurality of delay times provides a user configurable delay of said second setup/hold window relative to said transition of said clock signal (Col. 5, lines 65-67).

However, while Conn teaches a sample absolute value of the delay times and that the delay times may be modified (Col. 3, lines 45-60), Conn is silent regarding the size of the delay times in comparison with the period of a clock signal. Dallas teaches a programmable delay in which each of said plurality of delay times is less than a period of a clock signal (Table 2 on page 4, maximum delay for DS1020-15 is 48.25 ns; AC Electrical Characteristics on page 6, minimum clock width is 50 ns). At the time of the invention, it would have been obvious to apply the details of Dallas' programmable delay to Conn's apparatus. A motivation for doing so would have been "to satisfy the requirements of a particular application" (Conn, Col. 3, lines 45-60).

As per claim 13, Conn teaches storing said delayed data signal and presenting a data output signal in response to said clock signal (Fig. 1, at flip-flop 510A)

As per claim 15, Conn teaches presenting a first signal (Fig. 2, at input node 230) in response to said data signal.

As per claim 16, Conn teaches presenting one or more output delay signals response to said first signal (Fig. 2, from delay elements 240-246).

As per claim 17, Conn teaches presenting receiving said one or more output delay signals and presenting said delayed data signal (Fig. 2, at multiplexer 250).

As per claims 18-20, Conn teaches switching one or more output signals in response to a user configuration signal (Fig. 2, input terminals 235).

6. Claims 4-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Conn/Dallas as applied to claim 1 above, and further in view of JEDEC Standard No. 8-6, "High Speed Transceiver Logic (HSTL) - A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits", EIA/JESD8-6, August 1995 (hereinafter "JEDEC").

As per claim 4, while Conn/Dallas teaches presenting a first signal in response to a data input, Conn/Dallas does not expressly teach that said first circuit further comprises an HSTL circuit. HSTL is one of multiple transmission logic specifications in common use. It would have been a matter of design to have the first circuit conform to the JEDEC standard. Therefore at the time of the invention, it would have been obvious to one of ordinary skill in the art to apply the JEDEC standard to Conn/Dallas's apparatus.

As per claims 5-10, since Conn/Dallas teaches the method of claims 15-20, Con/Dallas/JEDEC teaches the claimed apparatus.

7. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Conn/Dallas as applied to claim 1 above, and further in view of Olson, U.S. Patent No. 5,247,617.

As per claim 22, Conn/Dallas does not expressly teach the apparatus comprising a FIFO memory. Olson teaches replacing a register with a FIFO (Col. 1, lines 42-47). At the time of the invention, it would have been obvious to one of ordinary skill in the art to

replace to Conn/Dallas's register (Fig. 5, flip-flop 510A) with Olson's FIFO. A motivation for doing so would have been to reduce processing overhead (Olson, col. 1, line 42-47).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. After the move in October, the new telephone number will be 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

aw
August 26, 2003

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